FIG. _1
(PRIOR ART)

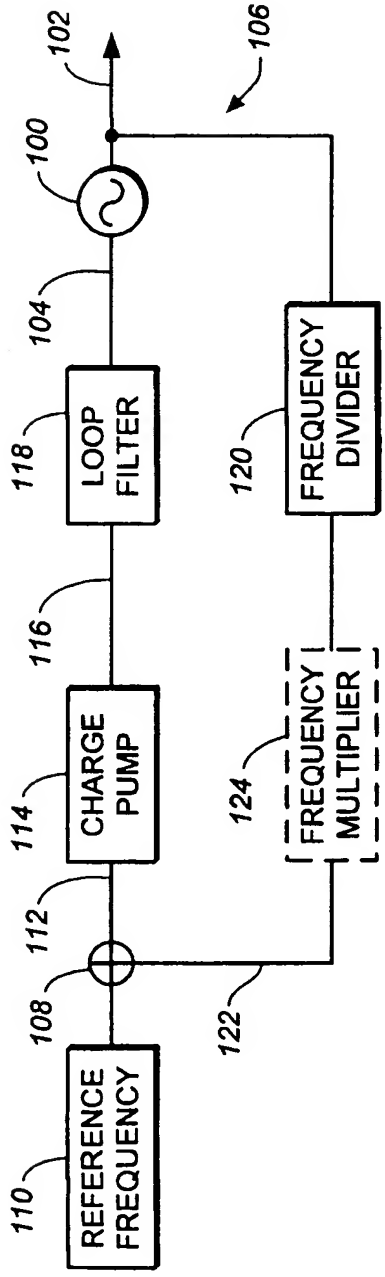


FIG. _2

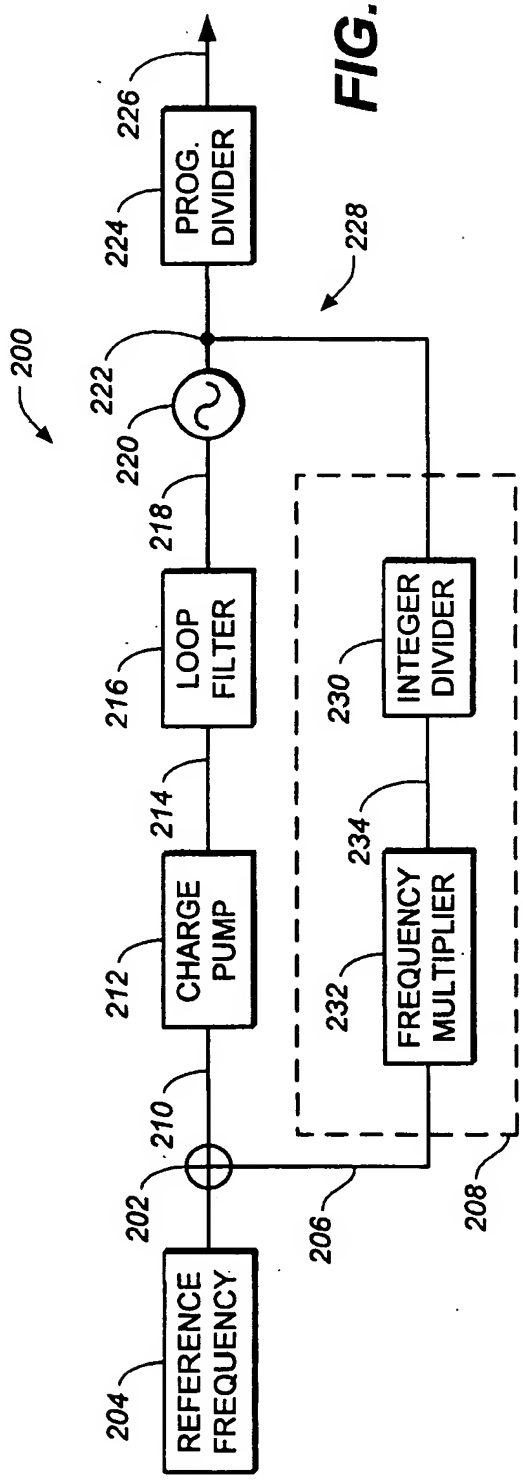


FIG. _ 3

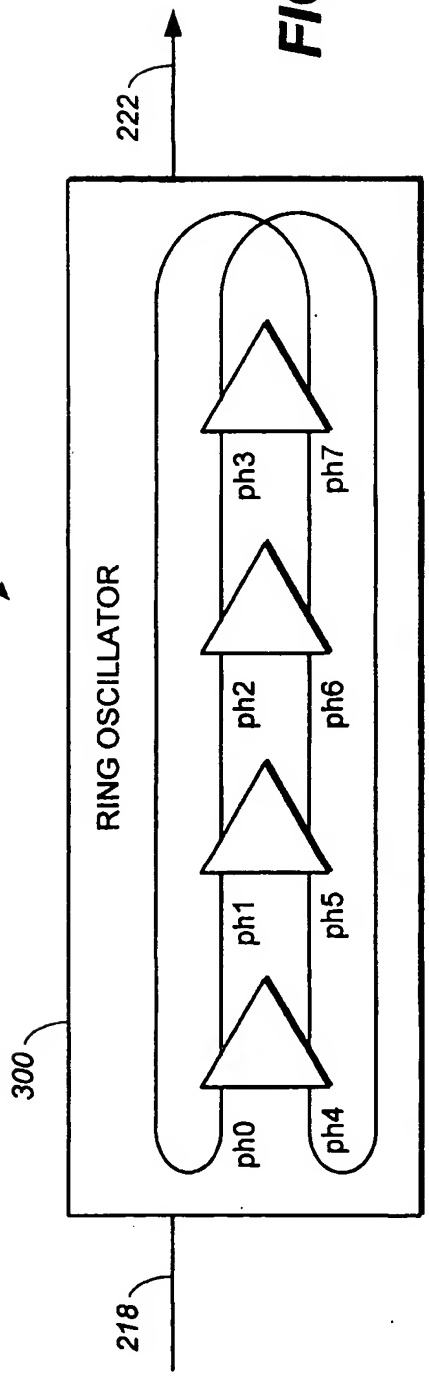
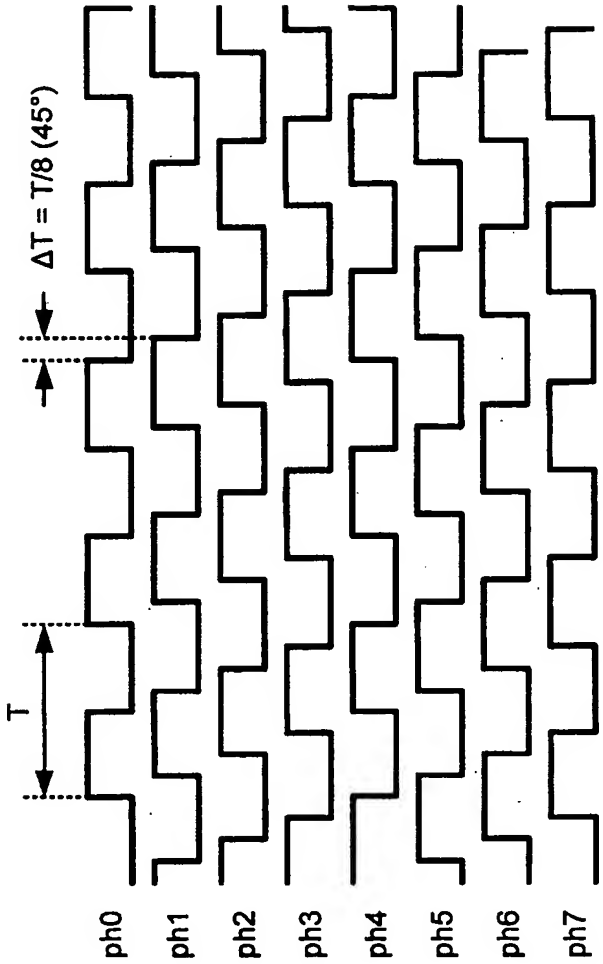

220
222
RING OSCILLATOR
300
218
ph0
ph1
ph2
ph3
ph4
ph5
ph6
ph7

FIG. _4


ΔT = T/8 (45°)
T
ph0
ph1
ph2
ph3
ph4
ph5
ph6
ph7

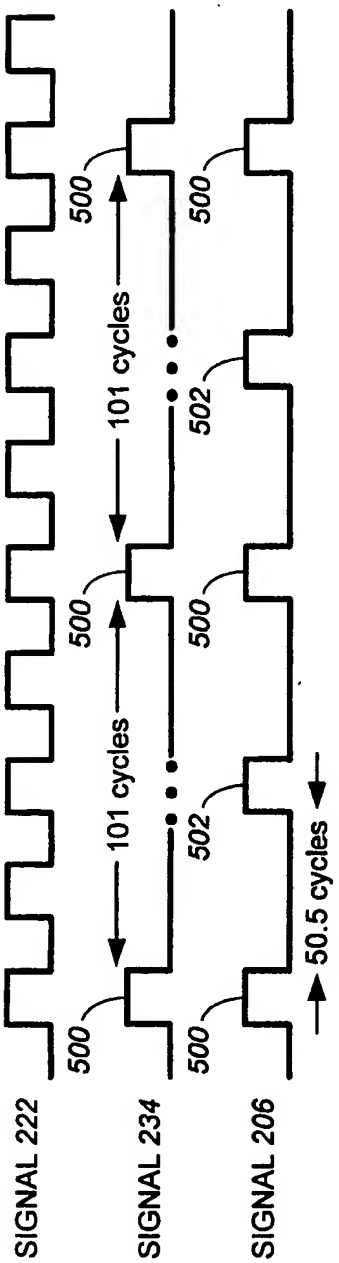

SIGNAL 222
SIGNAL 234
SIGNAL 206
500
502
101 cycles
50.5 cycles

FIG. _ 5

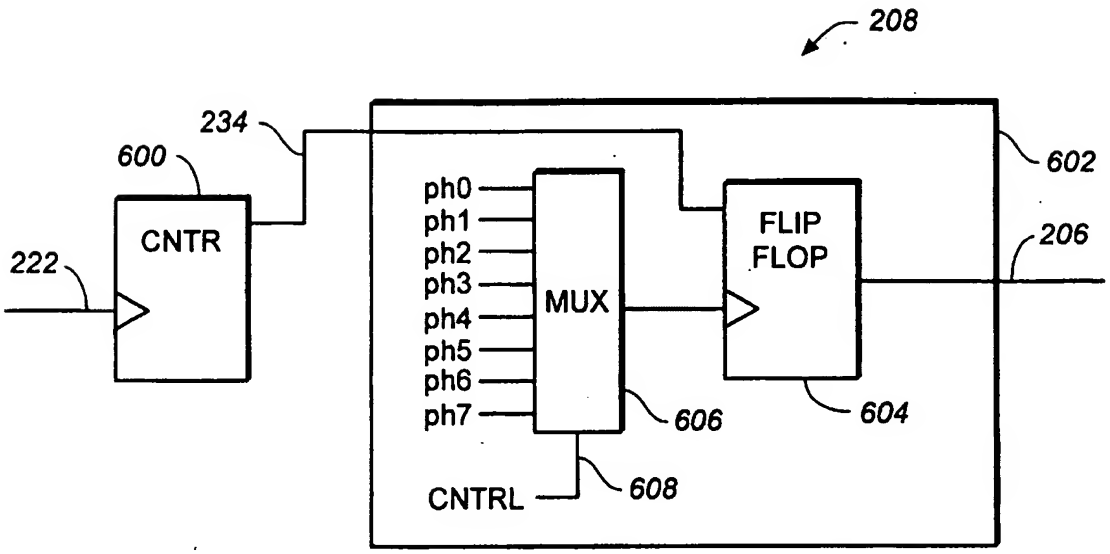

208
234
600
602
CNTR
222
ph0
ph1
ph2
ph3
ph4
ph5
ph6
ph7
MUX
FLIP
FLOP
206
606
604
CNTRL
608

FIG. _ 6

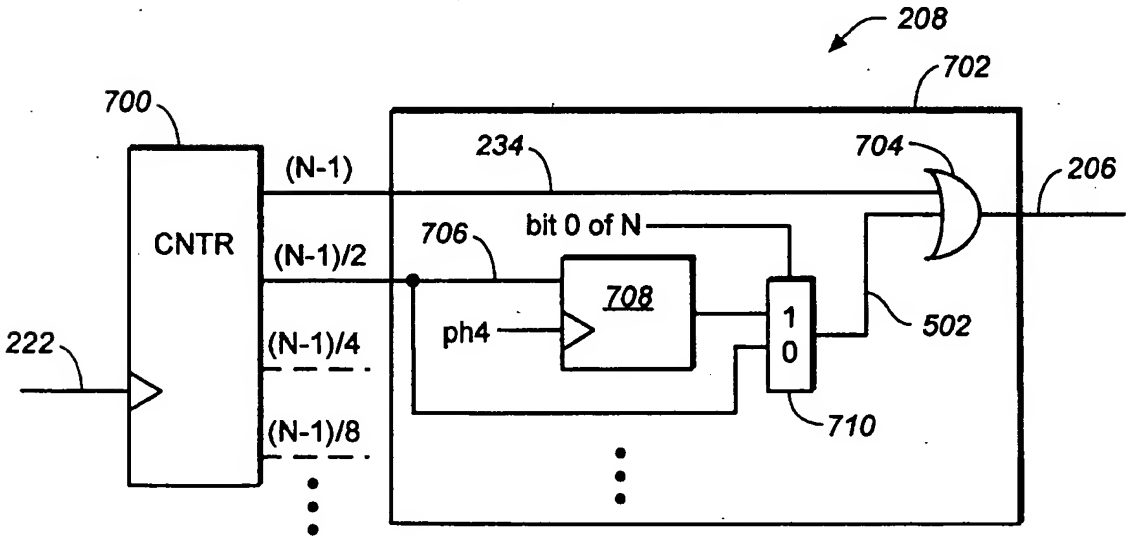

208
702
700
234
704
206
(N-1)
CNTR
706
bit 0 of N
(N-1)/2
708
ph4
1
0
502
222
(N-1)/4
(N-1)/8
710

FIG. _ 7

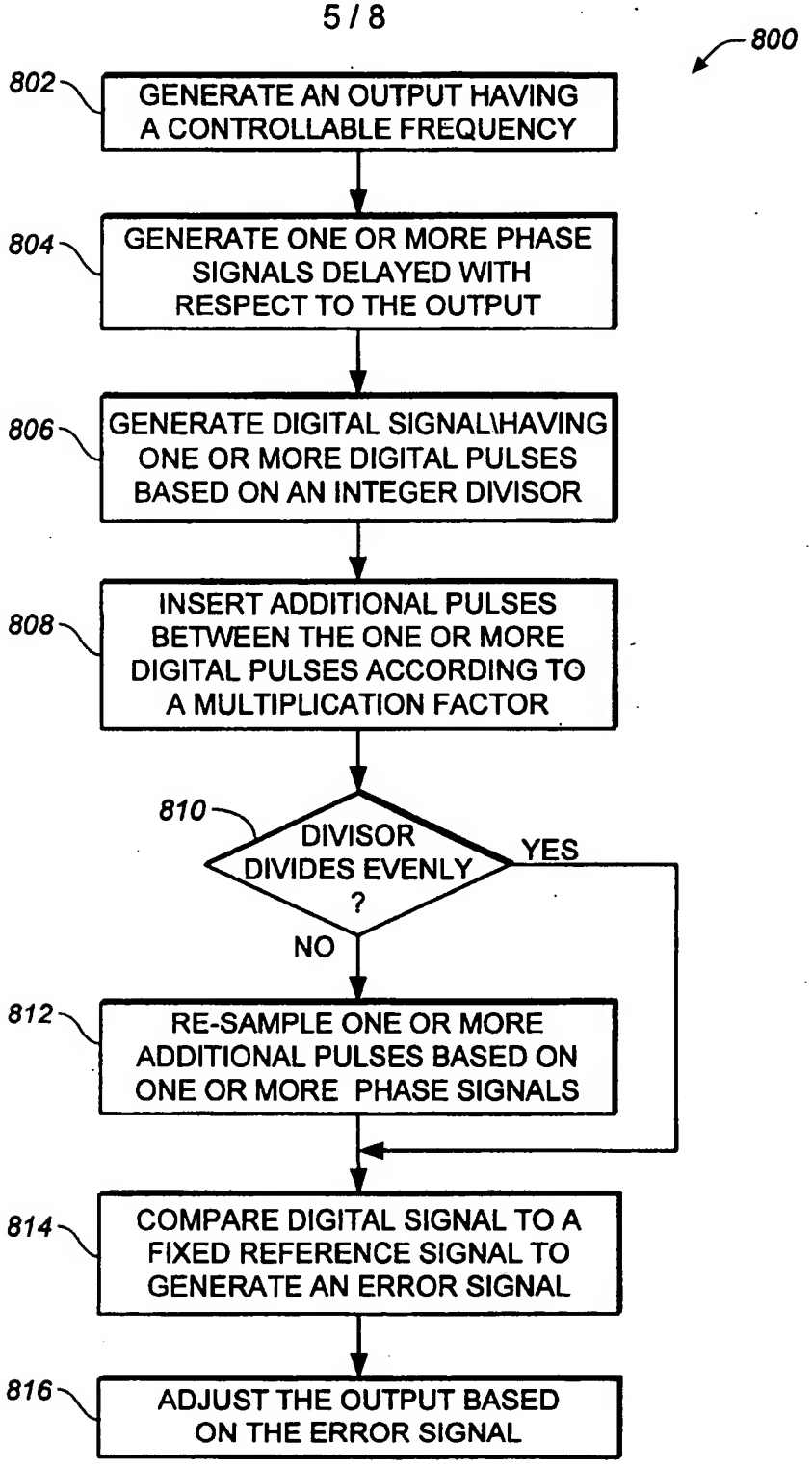

800
802
GENERATE AN OUTPUT HAVING A CONTROLLABLE FREQUENCY
804
GENERATE ONE OR MORE PHASE SIGNALS DELAYED WITH RESPECT TO THE OUTPUT
806
GENERATE DIGITAL SIGNAL\HAVING ONE OR MORE DIGITAL PULSES BASED ON AN INTEGER DIVISOR
808
INSERT ADDITIONAL PULSES BETWEEN THE ONE OR MORE DIGITAL PULSES ACCORDING TO A MULTIPLICATION FACTOR
810
DIVISOR DIVIDES EVENLY ?
YES
NO
812
RE-SAMPLE ONE OR MORE ADDITIONAL PULSES BASED ON ONE OR MORE PHASE SIGNALS
814
COMPARE DIGITAL SIGNAL TO A FIXED REFERENCE SIGNAL TO GENERATE AN ERROR SIGNAL
816
ADJUST THE OUTPUT BASED ON THE ERROR SIGNAL

FIG. _8

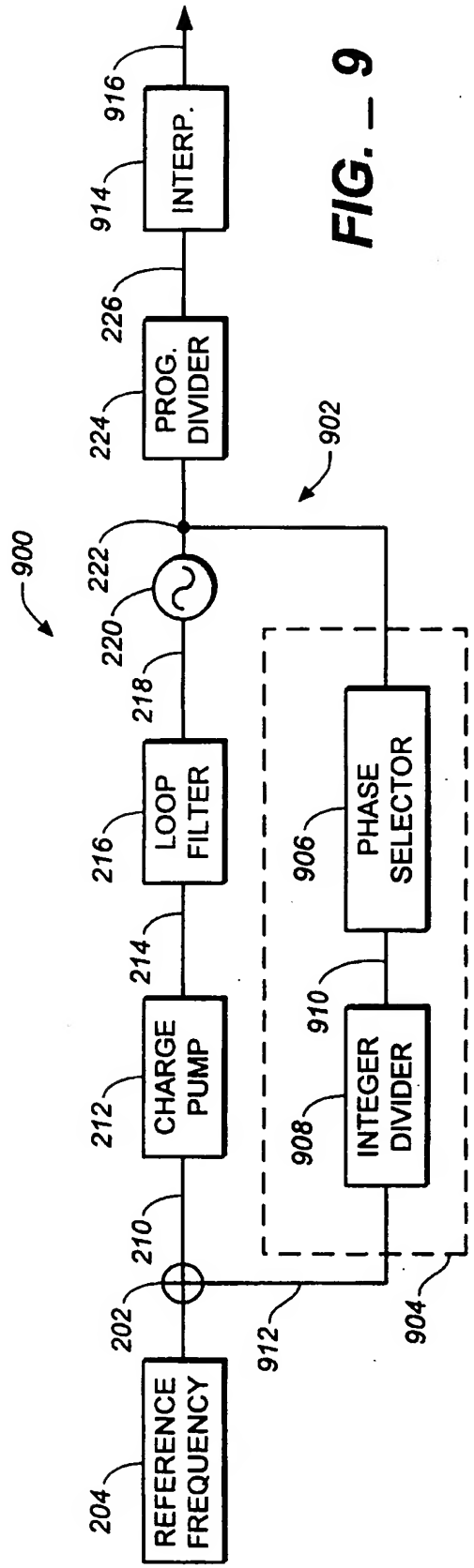

900
902
REFERENCE FREQUENCY
204
202
210
CHARGE PUMP
212
214
LOOP FILTER
216
218
220
222
PROG. DIVIDER
224
226
INTERP.
914
916
INTEGER DIVIDER
908
910
PHASE SELECTOR
906
912
904

FIG. _ 9

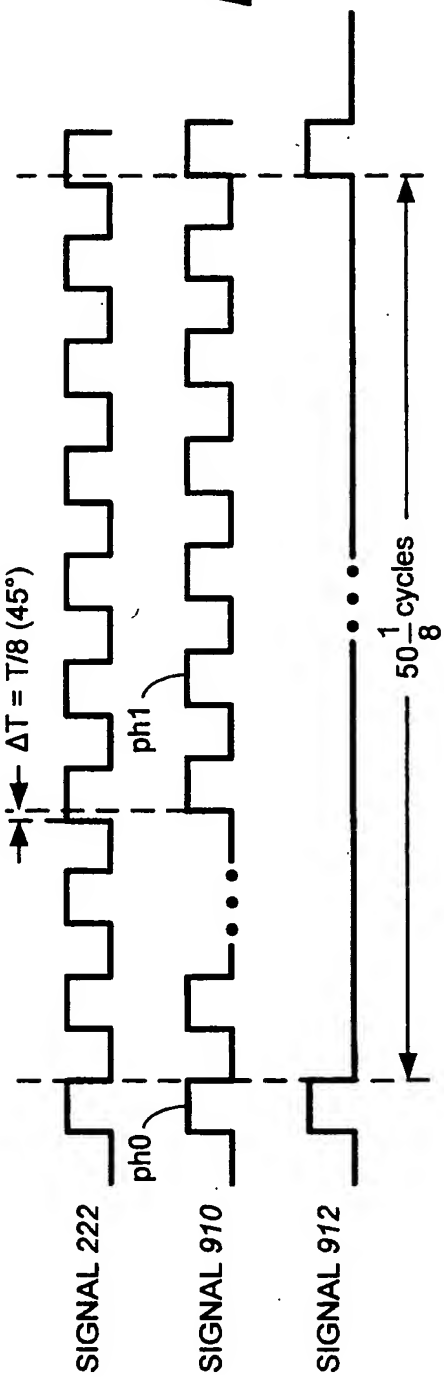

ΔT = T/8 (45°)
ph1
ph0
SIGNAL 222
SIGNAL 910
SIGNAL 912
50 1/8 cycles

FIG. _ 10

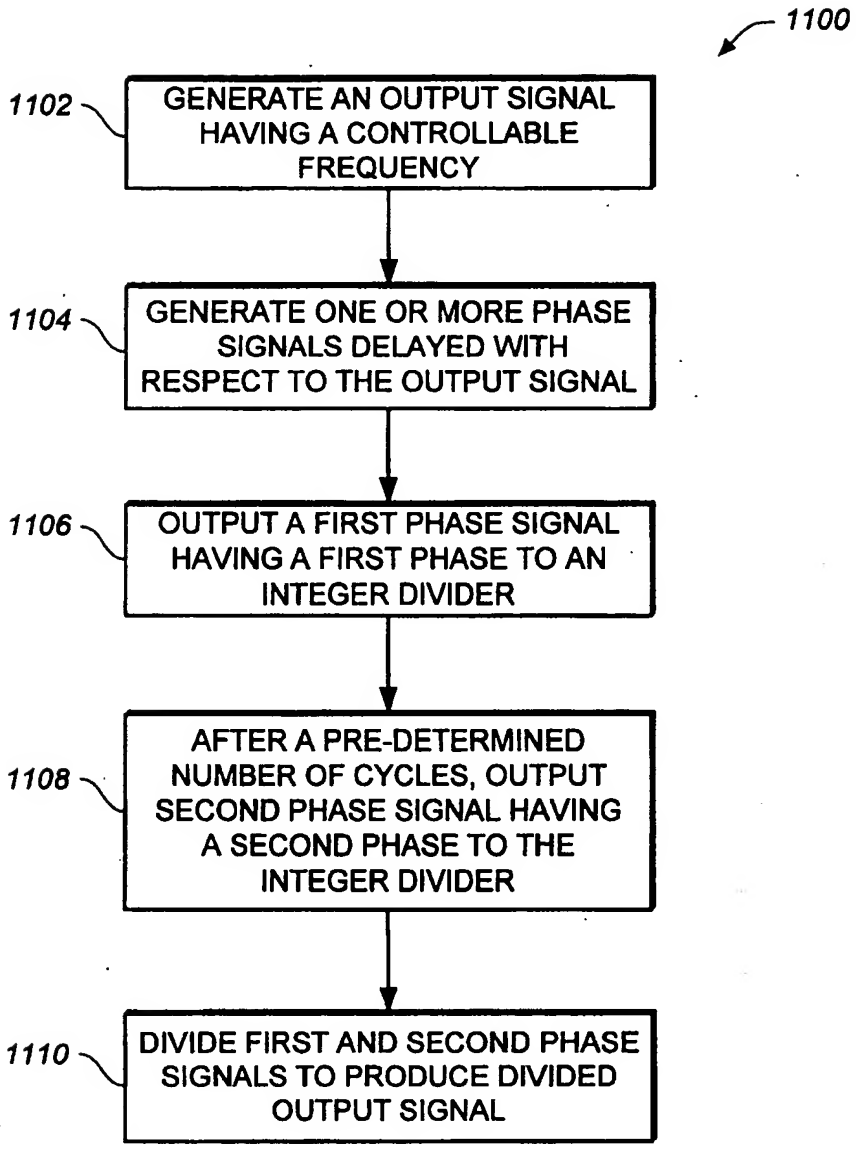

1100
1102
GENERATE AN OUTPUT SIGNAL HAVING A CONTROLLABLE FREQUENCY
1104
GENERATE ONE OR MORE PHASE SIGNALS DELAYED WITH RESPECT TO THE OUTPUT SIGNAL
1106
OUTPUT A FIRST PHASE SIGNAL HAVING A FIRST PHASE TO AN INTEGER DIVIDER
1108
AFTER A PRE-DETERMINED NUMBER OF CYCLES, OUTPUT SECOND PHASE SIGNAL HAVING A SECOND PHASE TO THE INTEGER DIVIDER
1110
DIVIDE FIRST AND SECOND PHASE SIGNALS TO PRODUCE DIVIDED OUTPUT SIGNAL

FIG. _ 11

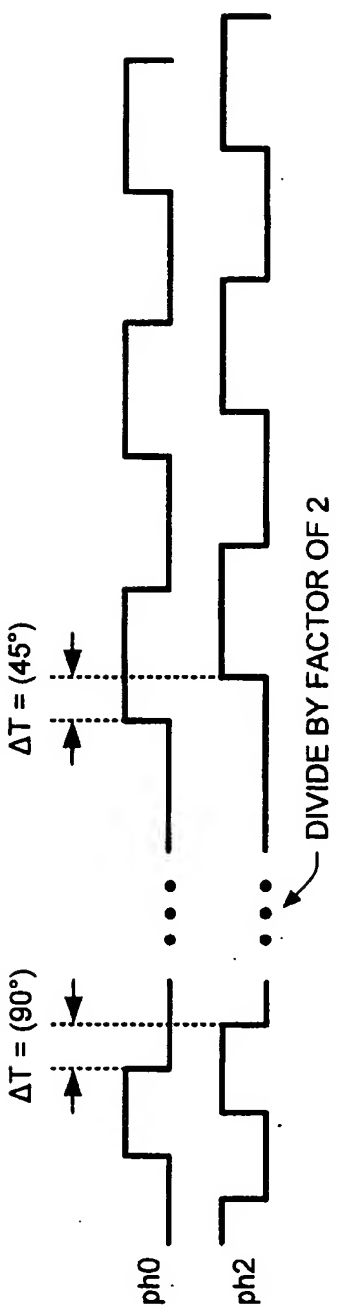

ΔT = (45°)
ΔT = (90°)
DIVIDE BY FACTOR OF 2
ph0
ph2

FIG. _ 12

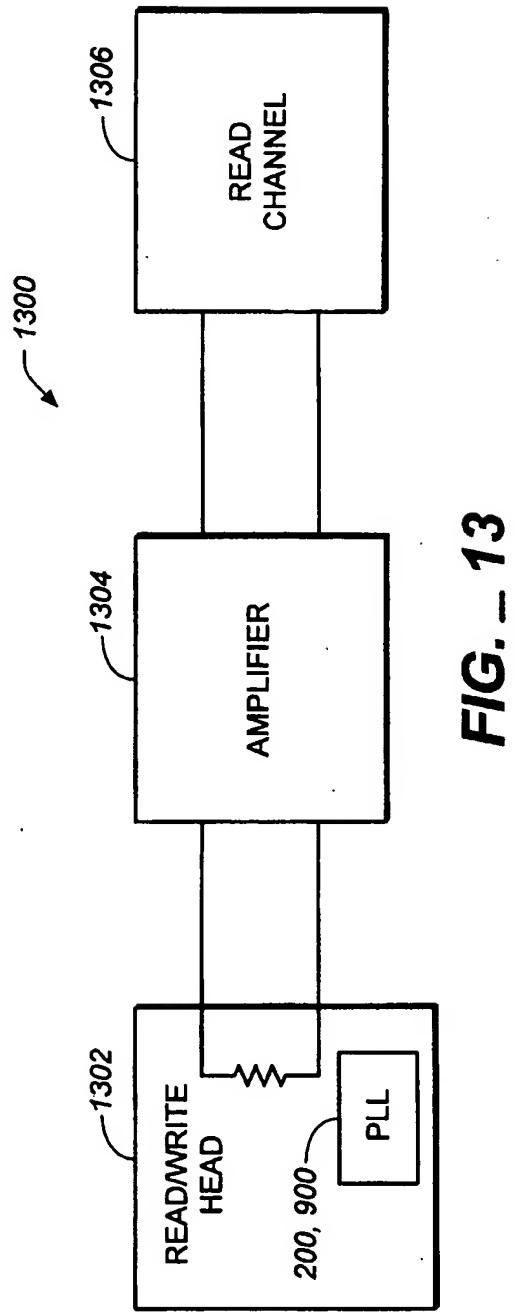

1300
1306
READ CHANNEL
1304
AMPLIFIER
1302
READ/WRITE HEAD
PLL
200, 900

FIG. _ 13